```
1   ----------------------------------------------------------------------------------
2   -- Company:
3   -- Engineer:
4   --
5   -- Create Date:    22:08:39 12/21/2015
6   -- Design Name:
7   -- Module Name:    test_board1 - Behavioral
8   -- Project Name:
9   -- Target Devices:
10  -- Tool versions:
11  -- Description:
12  --
13  -- Dependencies:
14  --
15  -- Revision:
16  -- Revision 0.01 - File Created
17  -- Additional Comments:
18  --
19  ----------------------------------------------------------------------------------
20  library IEEE;
21  use IEEE.STD_LOGIC_1164.ALL;
22  use IEEE.STD_LOGIC_ARITH.ALL;
23  use IEEE.STD_LOGIC_UNSIGNED.ALL;
24
25  ---- Uncomment the following library declaration if instantiating
26  ---- any Xilinx primitives in this code.
27  --library UNISIM;
28  --use UNISIM.VComponents.all;
29
30  entity test_board1 is
31      Port ( clk  : in   STD_LOGIC;
32             in1  : in   STD_LOGIC;
33             in2  : in   STD_LOGIC;
34             in3  : in   STD_LOGIC;
35             in4  : in   STD_LOGIC;
36             in5  : in   STD_LOGIC;
37             in6  : in   STD_LOGIC;
38             in7  : in   STD_LOGIC;
39             in8  : in   STD_LOGIC;
40             led1 : out  STD_LOGIC;
41             led2 : out  STD_LOGIC;
42             led3 : out  STD_LOGIC;
43             led4 : out  STD_LOGIC;
44             out1 : out  STD_LOGIC;
45             out2 : out  STD_LOGIC;
46             out3 : out  STD_LOGIC);
47  end test_board1;
48
49  architecture Behavioral of test_board1 is
50     signal CLK_DIV : std_logic_vector (21 downto 0);
51     signal clk2    : STD_LOGIC;
52     signal regi    : std_logic_vector (3 downto 0);
53     signal lines   : std_logic_vector (7 downto 0);
54
55  begin
56
57     DIVIDER: process (clk)
58     begin
59       if rising_edge(clk) then
60           CLK_DIV <= CLK_DIV + '1';
61           if CLK_DIV = "11111111111111111111" then
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```
 62                   clk2 <= not clk2;                          -- Secound Clock = Master / 2^2
 63                end if;
 64                lines(0) <= in1;
 65                lines(1) <= in2;
 66                lines(2) <= in3;
 67                lines(3) <= in4;
 68                lines(4) <= in5;
 69                lines(5) <= in6;
 70                lines(6) <= in7;
 71                lines(7) <= in8;
 72             end if;
 73          end process DIVIDER;
 74
 75          SHIFT_PROC: process (clk2)
 76          begin
 77             if rising_edge(clk2) then
 78       --          regi(0) <= lines(0);
 79       --          regi(1) <= lines(1);
 80       --          regi(2) <= lines(2);
 81       --          regi(3) <= lines(3);
 82                if regi = "0000" then
 83                   regi <= "1000";
 84                elsif lines = "00000000" then
 85                   regi <= "1000";
 86                elsif lines = "11111110" then
 87                   regi <= "1000";
 88                elsif lines = "11111101" then
 89                   regi <= "1100";
 90                elsif lines = "11111011" then
 91                   regi <= "1110";
 92                elsif lines = "11110111" then
 93                   regi <= "1111";
 94                elsif lines = "11101111" then
 95                   regi <= "1010";
 96                elsif lines = "11011111" then
 97                   regi <= "0101";
 98                elsif lines = "10111111" then
 99                   regi <= "1001";
100                elsif lines = "01111111" then
101                   regi <= "0110";
102                else
103                   regi(0) <= regi(3);
104                   regi(1) <= regi(0);
105                   regi(2) <= regi(1);
106                   regi(3) <= regi(2);
107                end if;
108             end if;
109          end process SHIFT_PROC;
110
111          led1 <= regi(0);
112          led2 <= regi(1);
113          led3 <= regi(2);
114          led4 <= regi(3);
115
116          out1 <= '0';
117          out2 <= '0';
118          out3 <= '0';
119
120       end Behavioral;
121
122
```